

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A data transmission line, used continuously, connected in a plurality of stages in an asynchronous system, comprising:

a data holding unit receiving and holding data transmitted from a preceding stage or data output from an external synchronous system, and outputting and transmitting the data received and held to a succeeding stage;

B a transfer control unit for controlling input and output of said data at said data holding unit; and

an adjustment unit for adjusting timing of input of one of the data output from said synchronous system and the data transmitted, in the asynchronous system from said preceding stage to said data holding unit, by said transfer control unit, when a mode in which (data output from said synchronous system is taken and transmitted to said data transmission line.


2. (Original) The data transmission line according to claim 1, further comprising

buffer means controlled by said synchronous system,

said buffer means provided between said synchronous system and said data holding unit, receiving and temporarily holding output

data of said synchronous system and outputting the data to said data holding unit.

3. (Original) The data transmission line according to claim 2, wherein said mode designation is canceled in response to completion of data input to said data holding unit.

 4. (Original) The data transmission line according to claim 3, wherein

said transfer control unit includes, in order to transfer a first pulse applied from said preceding stage as a second pulse to said succeeding stage, in accordance with an instruction signal instructing transfer acknowledgement or inhibition,

first storage means for storing said first pulse,

a second storage means reset in response to inhibition state of said instruction signal,

third storage means reset in response to an input of said first pulse and reset in response to an arbitrary applied third pulse input, and

logic means for outputting a fourth pulse in response to a fact that said first storage means is storing said first pulse, said first pulse is not being applied to said first storage means,

said second storage means is reset, said instruction signal is in acknowledged state, and said third storage means is reset,

said first storage means being reset by an input of said fourth pulse, said second storage means storing said fourth pulse and generating said second pulse; and

*21 Cont.* said adjustment unit generates, in response to a fact that said first storage means stores said first pulse and said first pulse is not being applied to said first storage means, said third pulse with a desired timing between data transfer of said asynchronous system and a clock of said synchronous system.

5. (Original) The data transmission line according to claim 4, wherein said data holding unit includes an asynchronous holding circuit for holding data transmitted in said asynchronous system, and a synchronous holding circuit for holding data output from said synchronous system.

6. (Original) The data transmission line according to claim 5, wherein said asynchronous system includes a data driven type information processing unit, and said synchronous system includes a clock synchronous information processing unit.

7. (Original) The data transmission line according to claim 1, wherein said mode designation is canceled in response to completion of input to said data holding unit.

8. (Original) The data transmission line according to claim 7, wherein said transfer control unit includes, in order to transfer a first pulse applied from said preceding stage as a second pulse to said succeeding stage, in accordance with an instruction signal instructing transfer acknowledgement or inhibition,

first storage means for storing said first pulse,

a second storage means reset in response to inhibition state of said instruction signal,

third storage means reset in response to an input of said first pulse and reset in response to an arbitrary applied third pulse input, and

logic means for outputting a fourth pulse in response to a fact that said first storage means is storing said first pulse, said first pulse is not being applied to said first storage means, said second storage means is reset, said instruction signal is in acknowledged state, and said third storage means is reset,

said first storage means being reset by an input of said fourth pulse, said second storage means storing said fourth pulse and generating said second pulse; and

said adjustment unit generates, in response to a fact that said first storage means stores said first pulse and said first pulse is not being applied to said first storage means, said third pulse with a desired timing between data transfer of said asynchronous system and a clock of said synchronous system.

9. (Original) The data transmission line according to claim 1, wherein

said transfer control unit includes, in order to transfer a first pulse applied from said preceding stage as a second pulse to said succeeding stage, in accordance with an instruction signal instructing transfer acknowledgement or inhibition,

first storage means for storing said first pulse,

a second storage means reset in response to inhibition state of said instruction signal,

third storage means reset in response to an input of said first pulse and reset in response to an arbitrary applied third pulse input, and

logic means for outputting a fourth pulse in response to a fact that said first storage means is storing said first pulse,

said first pulse is not being applied to said first storage means, said second storage means is reset, said instruction signal is in acknowledged state, and said third storage means is reset,

*Pl. Cont.* said first storage means being reset by an input of said fourth pulse, said second storage means storing said fourth pulse and generating said second pulse; and

said adjustment unit generates, in response to a fact that said first storage means stores said first pulse and said first pulse is not being applied to said first storage means, said third pulse with a desired timing between data transfer of said asynchronous system and a clock of said synchronous system.

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